

IN THE CLAIMS

What is claimed is:

- 1 **1.** A monitoring structure, comprising:
 - 2 at least one monitoring trench formed through a first layer and
 - 3 terminating at a second layer; and
 - 4 a feature formed in, with, or in relation to the monitoring trench that
 - 5 are configured to monitor at least one process step that forms corresponding
 - 6 features in, with, or in relation to non-monitoring trenches in a different layer
 - 7 than the first layer.
- 1 **2.** The monitoring structure of claim 1, wherein:
 - 2 the first layer includes a deposited layer of a predetermined thickness.
- 1 **3.** The monitoring structure of claim 1, wherein:
 - 2 the first layer comprises polysilicon; and
 - 3 the different layer comprises an essentially monocrystalline silicon
 - 4 wafer substrate.
- 1 **4.** The monitoring structure of claim 1, wherein:
 - 2 the first layer comprises silicon formed over a non-semiconductor-on-
 - 3 insulator (SOI) wafer substrate; and
 - 4 the different layer comprises a silicon layer formed over a substrate insulating

5 layer on a SOI wafer substrate.

1 5. The monitoring structure of claim 1, wherein:

2 the second layer comprises silicon dioxide.

1 6. The monitoring structure of claim 1, wherein:

2 the second layer comprises an etch stop layer and forms a bottom of
3 the at least one monitor trench.

1 7. The monitoring structure of claim 1, wherein:

2 the trenches formed in a different layer are shallow trench isolation
3 (STI) structures formed in an integrated circuit substrate; and
4 the at least one step includes a planarization step and the feature
5 includes a step height of a STI insulator material.

1 8. The monitoring structure of claim 7, wherein:

2 the planarization step includes chemical-mechanical polishing.

1 9. The monitoring structure of claim 1, wherein:

2 the trenches formed in a different layer are lateral island isolation
3 regions in a semiconductor-on-insulator substrate.

1 10. A method of forming a monitoring structure, comprising the steps of:
2 etching a first layer to form monitor trenches that extend through the
3 first layer and stop at an etch stop layer on a monitor wafer; and
4 forming a feature in, with, or in relation to the monitor trenches,
5 wherein a process to be monitored with said monitor structure forms a
6 corresponding non-monitor trench in a different layer or material than the first
7 layer.

1 11. The method of claim 10, further including:
2 the feature can vary according to a different trench depth; and
3 depositing a first layer to a predetermined thickness equivalent to a
4 desired trench depth.

1 12. The method of claim 11, further including:
2 forming an etch stop layer comprising silicon dioxide on a
3 semiconductor substrate; and
4 depositing the first layer includes depositing a layer comprising
5 polysilicon having a thickness less than 5000 angstroms.

1 13. The method of claim 10, further including:
2 the monitor wafer is a non semiconductor-on-insulator (SOI) wafer
3 and the normal wafer is a SOI wafer having semiconductor islands of a
4 predetermined thickness; and

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depositing a first layer of the predetermined thickness.

1 14. The method of claim 10, wherein:

2 etching the first layer includes forming a substrate trench etch mask on
3 the first layer.

1 15. The method of claim 10, wherein:

2 etching the first layer includes forming a substrate trench etch mask
3 pattern that essentially matches a semiconductor-on-insulator wafer lateral
4 island isolation pattern.

1 16. The method of claim 10, wherein:

2 etching the first layer includes substantially anisotropically etching
3 with a selectivity between the first layer and the second layer of greater than
4 30:1.

1 17. The method of claim 10, wherein:

2 forming a feature includes planarizing a trench insulator material that
3 extends inside the monitor trenches.

1 18. The method of claim 17, wherein:

2 planarizing includes chemical-mechanical polishing the trench
3 insulator material.

1 **20.** A method of monitoring a semiconductor manufacturing process, comprising the
2 steps of:

3 processing a monitor wafer having monitoring trenches formed in a
4 first layer of the monitoring wafer according to at least one process step that
5 forms a feature, the feature being formed in a non-monitoring wafer in, with,
6 or in relation to a different layer than the first layer in the semiconductor
7 manufacturing process.

1 **21.** The method of claim 20, wherein:

2 the first layer comprises a deposited layer and the different layer
3 comprises a wafer substrate.

1 **22.** The method of claim 20, wherein:

2 the first layer comprises a deposited layer and the different layer
3 comprises a semiconductor island layer formed over a semiconductor-on-
4 insulator wafer substrate.

1 **23.** The method of claim 20, wherein:

2 the at least one process step includes depositing and planarizing a
3 trench insulating material.

1 **24.** The method of claim 20, further including:

2 running the monitor wafer through the at least one process step with at

3 least one normal wafer.

1 **25.** The method of claim 20, further including:

2 the features include a trench insulator step height; and

3 examining the monitor structure in cross section to measure the

4 insulator step height.

1 **26.** The method of claim 25, wherein:

2 the at least one process step include a shallow trench isolation (STI)

3 insulator deposition step and a STI insulator chemical-mechanical polishing

4 step.